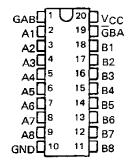
SDLS185

D2537, AUGUST 1979-REVISED MARCH 1988

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Local Bus-Latch Capability
- Hysteresis at Bus Inputs Improves Noise Margins
- · Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS620	3-State	Inverting
'L\$621	Open-Collector	True
4 6633	2 C+a+a	Truo

SN54LS620, SN54LS621, SN54LS622...J PACKAGE SN74LS620, SN74LS621, SN74LS623...DW OR N PACKAGE (TOP VIEW)



description

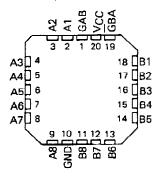
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}BA$ and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'LS620, 'LS621, and 'LS623 the capability to store data by simultaneous enabling of $\overline{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'LS621 and 'LS623 devices or complementary for the 'LS620.

SN54LS620, SN54LS621, SN54LS622 . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLE

ENABLE	INPUTS	OPERA	ATION
ĞBA	GAB	'LS620	'LS621, 'LS623
L	L	B data to A bus	B data to A bus
Н	H	A data to B bus	A data to B bus
Н	L	Isolation	Isolation
		B data to A bus,	B data to A bus,
L	H	A data to B bus	A data to B bus

H = high level, L = low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) .		 	 	 ,	7 V
Input voltage		 	 	 	7 V
Off-state output voltage					
Operating free-air temperature range:	SN54LS1	 	 	 	. –55°C to 125°C
	SN74LS'	 	 	 	0°C to 70°C
Storage temperature range					

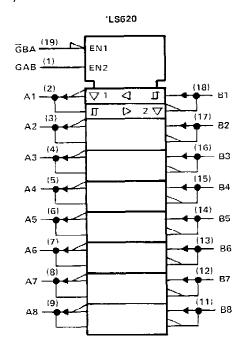
NOTE 1: Voltage values are with respect to network ground terminal.

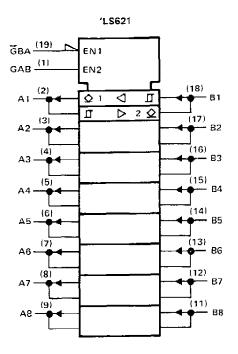
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

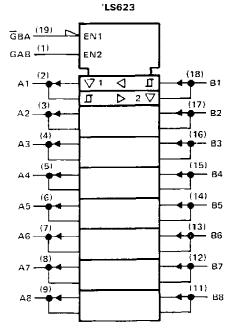


SN54LS620, SN54LS621, SN74LS620, SN74LS621, SN74LS623 OCTAL BUS TRANSCEIVERS

logic symbols†

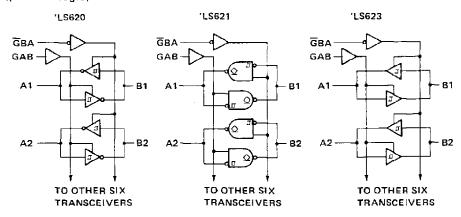




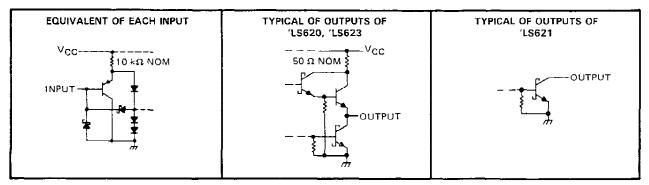


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

logic diagrams (positive logic)



schematics of inputs and outputs



SN54LS620, SN74LS620, SN74LS623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	Si	N54LS6	20		N74LS6 N74LS6		UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	<u></u>
Supply voltage, VCC (see Note 1)	4.5	5	5.5	4.75	5	5.25	_ v
High-level output current, IOH			-12			-15	πА
Low-level output current, IOL			12			24	mA_
Operating free-air temperature, To	-55		125	٥		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS†	SI	154LS6	20		N74LS6 N74LS6		UNIT
					MIN	TYP∓	MAX	MIN	TYP‡	MAX	
VIH	High-level input voltage				2			2			
VIL	Low-level input voltage						0.5			0.6	V
Vik	Input clamp voltage		V _{CC} = MIN,	l ₁ = –18 mA			-1.5			-1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or (3 input	V _{CC} = MIN		0.1	0.4		0.2	0.4		
			VCC = MIN,	I _{OH} = -3 mA	2.4	3.4		2.4	3.4		V
∨он	High-level output voltage		V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OH} = MAX	2			2			
			VCC = MIN,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	v
VOL	Low-level output voltage		V _{IH} = 2 V, V _{IL} = V _{IL} max	IQL = 24 mA			,		0.35	0.5	·
lozh	Off-state output current, high-level voltage applied		V _{CC} = MAX, V _O = 2.7 V	G at 2 V,			20			20	μА
lozL	Off-state output current, low-level voltage applied	•	V _{CC} = MAX, V _O = 0.4 V	G at 2 V,			-400			400	μΑ
	Input current at	A or B		V1 = 5.5 V			0.1			0.1	
Ц	maximum input voltage	GBA or GAB	VCC = MAX,	V1 = 7 V			0.1		•	0.1	mA
Чн	High-level input current		Vcc = MAX,	V ₁ = 2.7 V			20			20	μА
111	Law-level input current		V _{CC} = MAX,	V _I = 0.4 V			-0.4			-0.4	mA
los	Short-circuit output current §		VCC = MAX		-40		-225	-40		-225	mA
	1	Outputs high				48	70		48	70]
Icc	Total supply current	Outputs low	$V_{CC} = MAX$,	Outputs open		62	90		62	90	mA
~~	F	Outputs at Hi-Z]			64	95		64	95	

[†] For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

switching characteristics at VCC = 5 V, TA = 25°C

	PARAMETER	FROM	то	TEST CONDITIONS	,	LS620		SN	74LS6	23	UNIT
		(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	TYP	MAX	
	Propagation delay time,	Α	В			6	10		8	15	ns
₹₽LH	low-to-high-level output	В	Α	0 - 46 - 5		6	10		8	15	1113
	Propagation delay time,	A	В	C _L = 45 pF,		8	15		11	15	ns
[₹] PHL	high-to-low-level output	В	Α	D 007.0		8	15		11	15	1173
		бва	Α	R _L = 667 Ω,		31	40		31	40	ns
tbZr	Output enable time to low level	GAB	В	D 11 . 5		31	40		31	40	113
		GBA	Α	See Note 2		23	40		26	40	ns
^t PZH	Output enable time to high level	GAB	В			23	40		26	40	113
	0	ĞВА	А	0 5.5		15	25		15	25	
^t PLZ	Output disable time from low level	GAB	В	CL = 5 pF,		15	25		15	25	ns
	<u> </u>	Ğва	A	AL = 667 Ω,		15	25		15	25	
^t PHZ	Output disable time from high level	GAB	В	See Note 2		15	25		15	25	ns

 t_{PLH} = Propagation delay time, low-to-high-level output

tpZL = Output enable time to low level tpHZ = Output disable time from high level

tpLZ = Output disable time from low level



 $[\]ddagger$ All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

tpHL = Propagation delay time, high-to-low-level output tpZH = Output enable time to high level

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

PARAMETER	s	N54LS6	s	UNIT			
	MIN	NOM	MAX	MIN	NOM	MAX	1
Supply voltage, V _{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, VOH			5.5			5.5	V
Low-level output current, IOL			12			24	mA
Operating free-air temperature, TA	-55		125	0		70	·c

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS [‡]	S	N54LS6	521	SI	N74LS6	521	דואט
	Miss lauri in the second					TYP‡	MAX	MIN	ТҮР≑	MAX	
V_{IH}	High-level input voltage				2			2			V
VIL	Low-level input voltage	· <u> </u>					0.5			0.6	V
Vικ	înput clamp voltage		VCC = MIN,	I _I = -18 mA			1.5			-1.5	V
	Hysteresis (V _{T+} - V _{T-}) A	or B input	VCC = MIN		0.1	0.4		0.2	0.4		V
Іон	High-level output current		V _{CC} = MIN, V _{IL} = V _{IL} max,	•••			100			100	μА
Vol	Low-level output voltage		VCC = MIN,	I _{OL} = 12 mA		0.25	0.4		0,25	0.4	\ v
			V _{IL} ≈ V _{IL} max	IOL = 24 mA					0.35	0.5	
ı.	Input current at	A or B	1/ 1441/	5.5 V			0.1			0.1	^
Ц	maximum input voltage	GAB or GBA	$V_{CC} = MAX$,	V1 = 7 V		-	0.1			0.1	mA
¹1H	High-level input current		V _{CC} = MAX,	V ₁ = 2.7 V			20			20	μА
IL	Low-level input current	-	V _{CC} = MAX,	V _I = 0.4 V	Ī		-0.4			-0.4	: mA
lcc	Total supply current	Outputs high	V _{CC} = MAX,	Outputs open		48	70		48	70	mA
	rotal supply current	Total supply current Outputs low		Outpots open		62	90		62	90] '''

[†]For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

	PARAMETER	FROM	то	TEST CONDITIONS		'LS621		UNIT
	PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Propagation delay time,	A	В			17	25	
†PLH	low-to-high-level output	В	А			17	25	ns
	Propagation delay time,	A	В	1		16	25	
1PHL	high-to-law-level output	В	Α	$C_L = 45 \text{ pF},$		16	25	ns
	Output disable time	Ğва	А	R _L = 667 Ω, See Note 2		23	40	
[†] PLH	from law level	GAB	В	See Note 2		25	40	ns
	Output enable time	GBA	Α			34	50	
[†] PHL	from high level	GAB	В			37	50	ПБ

 $t_{\mbox{\scriptsize PLH}} = \mbox{\scriptsize Propagation delay time, low-to-high-level output}$

tpHL = Propagation delay time, high-to-low-level output

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

 $[\]ddagger$ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS623DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LS623NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS623DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LS623NSR	SO	NS	20	2000	346.0	346.0	41.0

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